

INTERNATIONAL JOURNAL OF ENGINEERING SCIENCES & MANAGEMENT FAULT IDENTIFICATION USING OF NN BASED GA PARAMETERS IN ANALOG CIRCUITS BY SIMULATION IMPLEMENTATION

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Abstract

The research titled as “Fault identification using of NN based GA parameters in analog circuits by simulation implementation” proposes a fault identification approach for analog circuit using hybrid evolutionary techniques and neural network in GA parameters. With the increasing demand for analog integrated circuit technology and the complexities and shrinking equipment dimensions, integrated circuit performance is becoming sensitive to inherent parameter deviations. Therefore fault detection and location in analog circuits have received more attention in recent decades. Fault detection in analog circuits is challenging due to poor circuit model, limited test nodes, component tolerance, non-linearity of output, limited access to internal nodes. The genetic algorithm is used as an evolutionary technique for the optimization and learning of neural networks. The proposed method has been validated through a state-variable filter circuit and all possible parametric variations have been derived for faulty and non-faulty conditions. A large area of research has been done on fault detection in analog circuits, but neural-network-based detection methods have proven to be more efficient as it has good robustness, adaptability, and learning capability. But neural networks have poor generalization capability and require a large number of iterations. So in this work, the boundaries of neural networks are overcome by designing a hybrid scheme of neural networks and evolutionary algorithms. All experiments are conducted on MATLAB R2015a. Experimental results are presented to show that the hybrid scheme is more efficient in terms of fault detection rate and time constraints than the neural network method.

Introduction

Fault is understood as any kind of malfunction in the system that leads to an unacceptable anomaly in the overall system performance. Fault identification is referred as detection of fault and its isolation. Faults detection and location in electronic equipment is one of the fundamental problems in production of reliable and safe electronic, multi-element systems. Generally digital circuits are part of all electronic system, the tendency of fault occurrence is in the analog part of the electronic system [1]. Despite many advances in design of analog

circuits, testing of these circuits remains a major problem. Fault detection in analog circuit is challenging due to poor fault modes, limited test nodes, component tolerance, non-linearity of outputs, limited internal nodes [2]. Single parametric and hard faults are the most common in discrete circuits [3].

Fault in analog circuit is consequence of failure of circuit. In electronic circuits, there exist different failure modes such as open circuits, short circuit, degraded performance and functional failures [4]. A failure mode is the effect by which failure is observed, while a failure mechanism is the chemical, physical, or metallurgical process, which leads to component failure [5]. Degradation faults depend mainly on parametric variation of the component used in a circuit.. This may be due to manufacturing defects, process variations, change in the environment or ambient temperature or wear out due to aging. While functional faults are based on the fact that a circuit may continue to function, but some of its performance specifications may lie outside their acceptable range. Faults in analog circuit are categorized as catastrophic fault and parametric fault [6].

Proposed Methodology

Fault detection in analog electronic circuit is complicated due to frequency dependent analog circuit response in most of the cases and non-accessibility of input nodes for testing purpose. The proposed methodology for fault identification involves preparation of fault dictionary for the circuit on which experimental validations has to be performed, and then neural network is developed with the input and target data from the CUT. Weights of the neural network are optimized by using genetic algorithm and then neural network is again developed with the optimized weights. Fault identification process is done on this optimized network. Flow diagram of methodology is shown in Figure 1 and all the steps are discussed in detail.

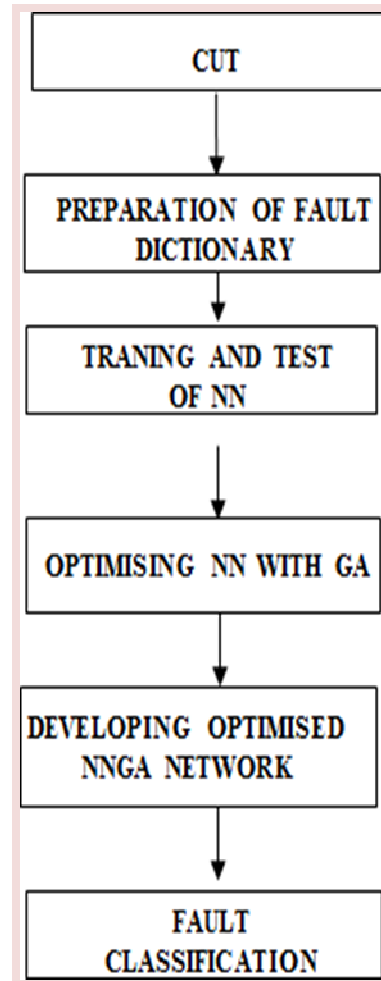


Figure 1: Flow diagram of proposed methodology

Preparation Of Fault Dictionary

To detect fault in analog circuit through parametric variation, first step is to prepare the fault dictionary for circuit under test i.e. CUT. The feature extracted from the circuit response should be unique for faulty and non- faulty case. The fault dictionary is the simplest form for mapping out which tests activate and propagate which faults. Fault dictionaries are made in the design stage for theoretical non- faulty circuits. They are then used in the identification stage to compare with experimental results on a failing circuit. Fault dictionary is prepared by extracting circuit response of the parameters of circuit under both faulty and non- faulty conditions.

1.1. Implementation Of Neural Network

Neural network is implemented by using neural network tool box of MATLAB software by giving one or more input samples, a bias, and an activation function. NN receives input, multiplies them by some random weight, the weighted sum of the input is then passes to a

function and produces an output. A Feed-forward back propagation type neural network is designed with ten numbers of neurons and one hidden layer. Network is trained by using Levenberg Marquardt back-propagation training function, it is the fastest back propagation algorithm and a first choice for supervised learning algorithm.

Training and Testing Of Neural Network

Neural network designed in the last step is ready to trained, to start with process the initial weights are randomly chosen and then the training or learning process of neural network begins. Supervised learning algorithm is utilised here. Weights are randomly assigned to the input layers and output is calculated, this process is repeated. Training with changing the random weights continues until best performance of neural network is achieved or until the minimum allowable sum square error is reached.

Optimizing NN With GA

Training of NN is an iterative process and it may take more time constraint. Neural network uses back propagation algorithm for training of network, this algorithm repeatedly trains the network until the output of the network is almost equal to the expected output. To overcome this long iterative process and to increase the fault detection rate of the network, Neural network is optimized with Genetic algorithm. Genetic algorithm is easy to implement in MATLAB using optimization toolbox. The range of random weights assigned to NN is optimized by GA to give the best possible combination of weights to NN which leads to better performance of the network.

DEVELOPING GA OPTIMIZED NN

Neural network is trained by the optimized weights found by genetic algorithm, this combination of optimized weights is capable to give the best performance of neural network. Thus it eliminates the iteration time to find the best combination of weight. Optimized neural network provides better performance with minimum possible error and thus the trained neural network is now ready for testing analog circuits for faults in the circuit.

FAULT DETECTION

Fault detection is by done comparing the output of the optimized neural network with the nominal values of the output ($\pm 5\%$ tolerance of nominal value) for the non-faulty condition. Deviation of output from the nominal values is referred to as fault in the circuit. Output of

neural network is set of component values of the circuit under test so we can easily detect the faulty component of the circuit, thus location of fault in circuit is also easily detectable

Experimental Result

Neural network is optimized with genetic algorithm in many possible ways by taking different parameters of genetic algorithm. Thus each time we get a different optimized neural network and the performance of each network is evaluated. Experiment is repeated with different crossover and selection functions of genetic algorithm. The result of genetic algorithm in each case is used to design an optimized neural network. This neural network performance is compared with neural network optimized with default parameters of GA. Performance and fault detection rate of neural networks optimized with different parameters of GA in each components of CUT is shown in Table 1. Network topology is considered as 4-10-9-9, number of epoch is 1000 and 3400 samples of data is taken.

In Table 4.1 BP is back propagation network without evolutionary algorithms while other Optimized neural networks with different GA parameters are named as:

- ❖ GABP- Default GA parameters (given in Table 3.2), Heuristic crossover function and stochastic uniform selection function.
- ❖ GABP1- single point crossover function.
- ❖ GABP2- Scattered crossover function.
- ❖ GABP3- Intermediate crossover function
- ❖ GABP4- Arithmetic crossover function.
- ❖ GABP5- Remainder selection function.
- ❖ GABP6- Uniform selection function.
- ❖ GABP7- Roulette selection function.
- ❖ GABP8- Tournament selection function

Table 1: Performance and fault detection rate of components of networks.

Network type	training time(sec)	R ₁ %	R ₂ %	R ₃ %	R ₄ %	R ₅ %	R ₆ %	R ₇ %	C ₁ %	C ₂ %
BP	17.84	73.73	73.72	73.714	73.50	73.70	73.77	73.488	73.81	73.30
GABP	94.97	90.06	84.80	86.75	87.18	89.41	86.23	85.38	86.57	87.37
GABP1	19.23	78.22	77.93	78.04	78.58	78.71	78.53	78.266	78.10	78.09
GABP2	31.04	87.02	84.15	86.55	86.3	86.56	85.39	84.72	86.3	86.48
GABP3	51.41	90.09	84.79	87.55	87.89	90.36	86.98	86.41	87.81	88.01
GABP4	28.02	81.66	81.31	82.11	82.29	82.18	81.99	82.19	82.02	82.28
GABP5	15.42	85.61	84.07	86.23	86.60	86.40	85.12	84.90	86.25	86.39
GABP6	11.92	74.44	73.90	73.94	73.63	74.21	74.23	74.28	74.46	74.58
GABP7	25.13	83.38	81.22	82.23	82.17	82.19	81.99	81.35	82.59	82.31
GABP8	19.86	82.06	81.11	82.54	82.66	82.25	81.49	81.44	82.15	82.34

From Table 4.1, GABP5 i.e. back propagation network optimized with genetic algorithm with parameter as remainder selection function is proved to be best in terms of fault detection rate and training time both. The validation performance of GABP5 and BP (Back propagation NN without optimizing with GA) is shown in Figure 4.2 and Figure 4.3 respectively and the regression graph of GABP5 neural network is shown in Figure 4.4.

Figure 2 and Figure 3 is plotted with respect to mean square error. Thus performance of the network is evaluated in terms of mean square error, therefore it should be minimum. GABP5 gives best validation performance at 0.035306 at epoch 525 and BP gives best validation performance at 0.091364 at epoch 5. Figure 4.4 is a regression graph of GABP5 which is plotted between output and target value. It gives the best training at $R=0.80296$, best validation at $R=0.78779$, best testing at $R=0.10986$ and overall best performance at

R=0.3239.

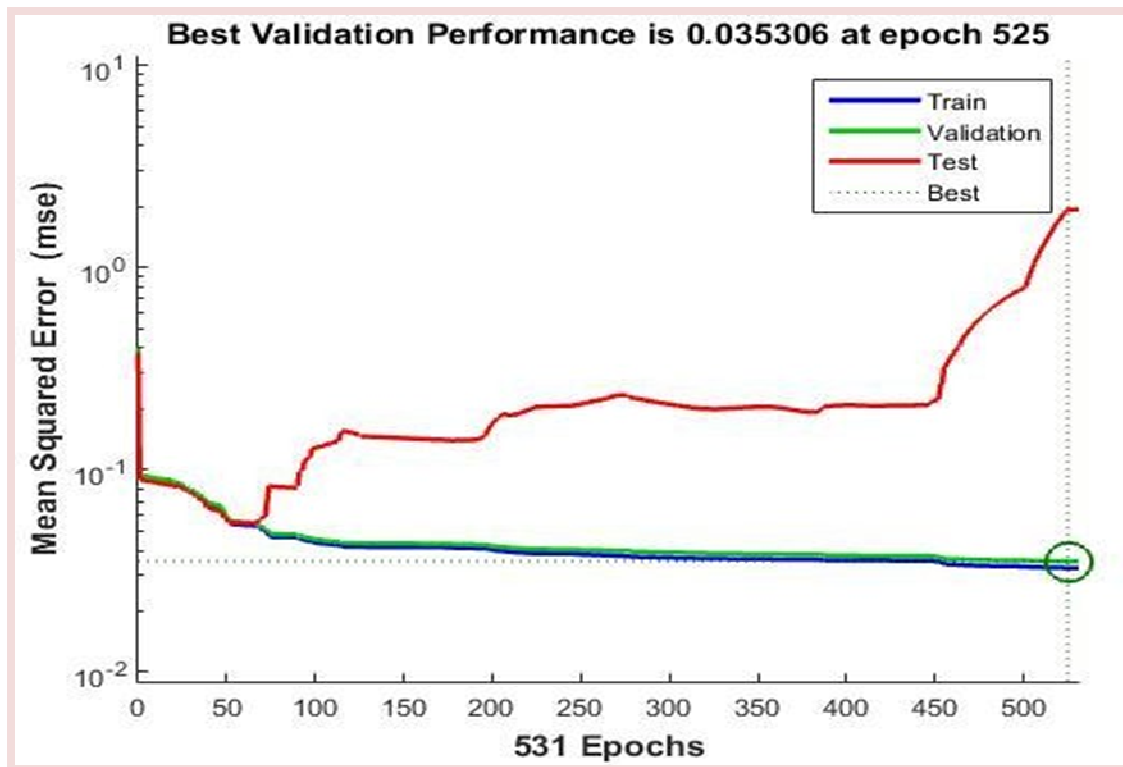


Figure 2: Validation performance graph of GABP5

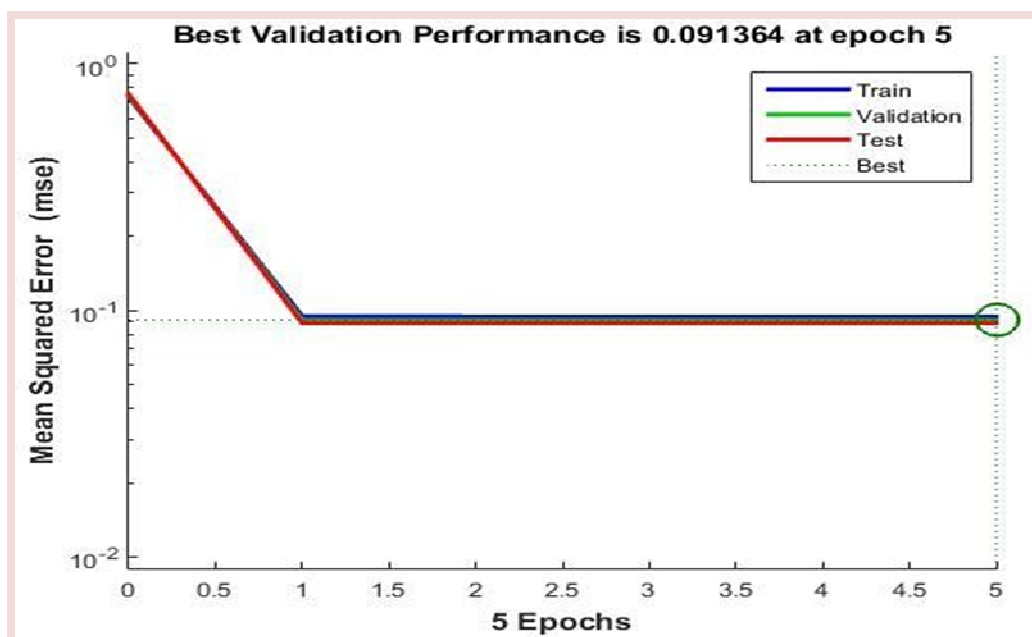


Figure 3: Validation performance graph of GABP

Analysis And Discussion

For training, testing and validation of network, 15% of data is taken for testing and training purpose each and 30% of data is taken for validation purpose. Overall fault detection rate and training time of each network with different parameters of genetic algorithm and back propagation neural network are given in Table 2.

Table 2: Fault detection rate of overall network and training time

Network type	Fault detection rate %	Training time (sec)
BP	73.63	17.84
GABP	87.08	94.97
GABP1	78.27	19.23
GABP2	84.94	31.04
GABP3	87.76	51.41
GABP4	82.00	28.02
GABP5	85.73	15.42
GABP6	74.18	11.92
GABP7	82.15	25.13
GABP8	82.00	19.86

Experiments shows that optimized neural network is giving better performance in terms of fault detection rate and training time of neural network as compare to the back-propagation neural network. Optimizing process of genetic algorithm is lengthy in terms of time constraint but once the genetic algorithm provides the optimized weights of neural network then neural network is trained and tested in very less time and works efficiently. From Table

2 comparison graph of different parameters based GA algorithms and BP algorithm in terms of fault detection rate and training time is shown in Figure 3.

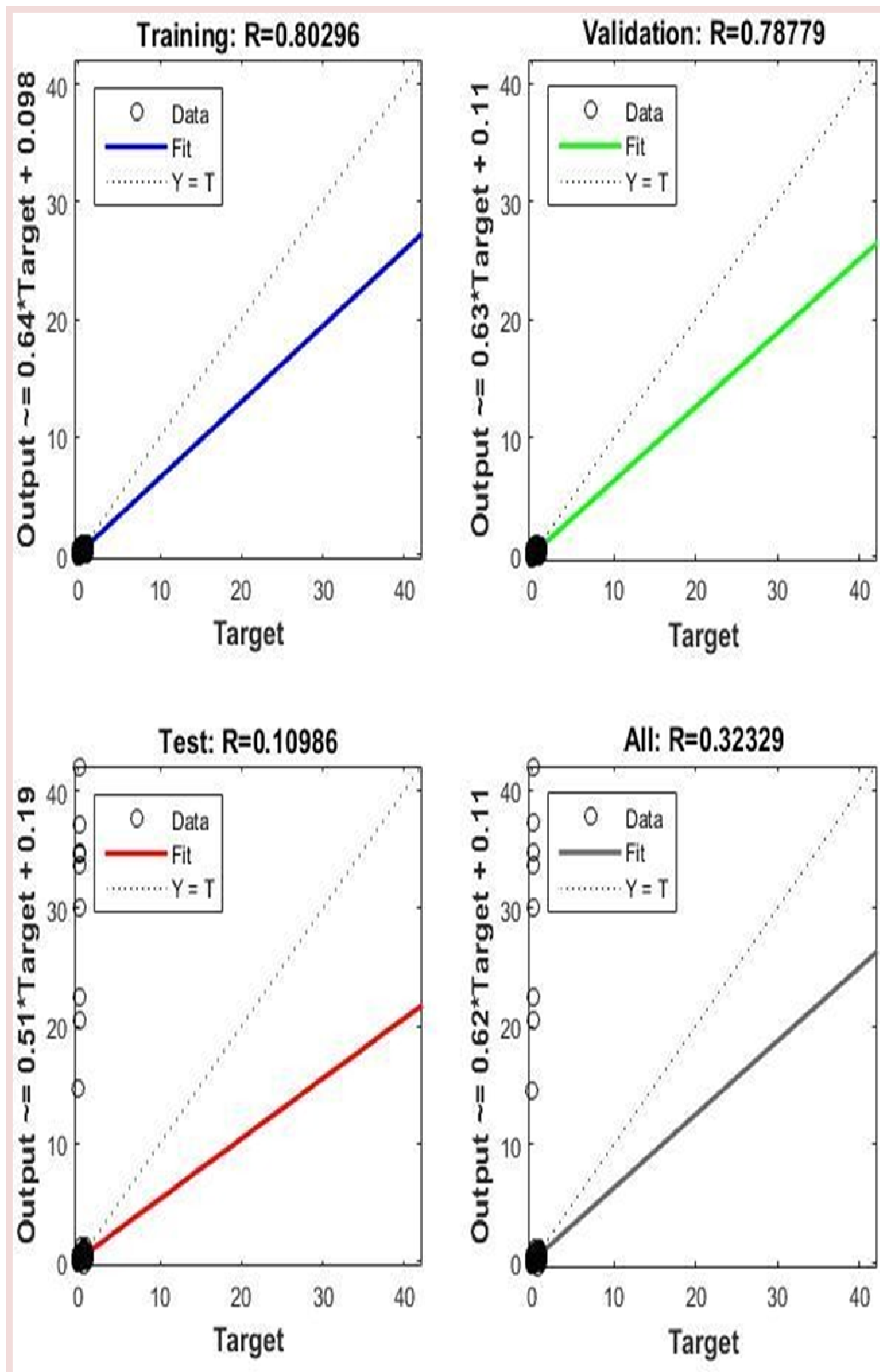


Figure 3: Regression graph of GABP5

Figure 4 is a comparative graph of proposed methodology with previous methodology [30] in terms of fault detection rate. Graph clearly shows that fault detection rate of proposed methodology i.e. GABP3 and GABP5 is 87.76% and 85.73% respectively which is better than the fault detection rate of previous methodology i.e. OWO-HWO (67%) and GA-BP (86%).

Table 3: Comparison of fault detection rate train time of different structure of network

Network topology	Training way	Number of epoch	Training time (s)	Fault location rate (%)
8-20-8	OWO-HWO	200	662	67
15-12-16	GA-BP	2000	24	86
4-10-9-9	GABP3	1000	51.41	87.76
4-10-9-9	GABP5	1000	15.42	85.73
4-10-9-9	GABP6	1000	11.92	74.18

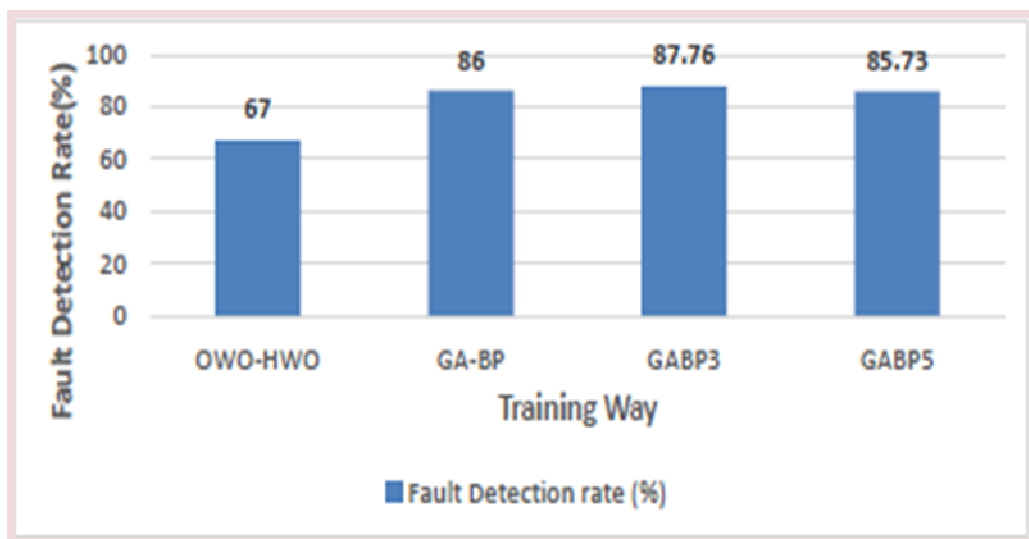


Figure 4: Comparative study graph of fault detection rate of proposed method with previous method

Conclusion

NN based GA method to detect faults in analog circuit is proposed and experimental validations have been carried out on state variable filter circuit. To enhance the performance of neural network and to overcome its limitations, initial weights of neural network are optimized using genetic algorithm. Neural network is optimized by using different parameters of genetic algorithm and performance of the different models of neural network has been compared to the back-propagation neural network and also compared to the neural network optimized by default parameters of genetic algorithm.

Thus a GA parametric network with a combination of maximum possible fault detection rate and minimum possible training time is preferable. In term of Fault detection rate GABP (default parameters) and GAPB3 (intermediate crossover function) networks gives the best performance while in terms of testing time GABP5 (Remainder selection function) and GABP6 (Uniform selection function) gives the best performance. Investigation of GA parameters shows that performance of network can be enhanced by using suitable parameters. This proposed hybrid neural network is capable to detect and locate soft faults in the analog circuits.

Reference

- [1].Deng, Y., He, Y., Sun, Y.(2010). Fault identification of analog circuits with tolerances using artificial neural networks. *IEEE Design & Test of Computers*, (pp. 292–295).
- [2].Jantos, Piotr, et al. "The influence of global parametric faults on analogue electronic circuits time domain response features." *Design and Diagnostics of Electronic Circuits and Systems*, 2008. DDECS 2008. 11th IEEE Workshop on. IEEE, 2008.
- [3].Maly, W., Strojwas, A. W., & Director, S. W. (1986). VLSI yield prediction and estimation: A unified framework. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 5, 114–130
- [4].Rahman, Md Mijanur, and T. Akter Setu. "An implementation for combining neural networks and genetic algorithms." *Int. J. Comput. Sci. Technol* 6.3 (2015).
- [5].Kavithamani, A., V. Manikandan, and N. Devarajan. "Analog circuit fault identification based on bandwidth and fuzzy classifier." *TENCON 2009-2009 IEEE Region 10*

Conference. IEEE, 2009.

- [6].Kavithamani, V. Manikandan and N. Devarajan, “Soft Fault Classification of Analog Circuits Using Network Parameters and Neural Networks” Springer Science+Business Media New York 2013, Received: 30 April 2012, Accepted: 8 March 2013, Published online: 11 April 2013, Pp. 237-240
- [7].Prithviraj Kabisatpathy, Alok Barua, and Satyabroto Sinha, “Fault Detection And Identification In Analog Integrated Circuits Using Artificial Neural Network In A Pseudorandom Testing Scheme” 3rd International Conference on Electrical & Computer Engineering ICECE 2004, 28-30 December 2004, Dhaka, Bangladesh, Pp. 52-55.
- [8].Sheikhan, Mansour, and Amir Ali Sha'bani. "PSO-optimized modular neural network trained by OWO-HWO algorithm for fault location in analog circuits." *Neural computing & applications* (2013): 1-12